In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Previously Presented) A system comprising:

a DAC that receives a multi-bit digital signal and outputs at least two analog signals including a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal, the second analog signal also being indicative of said sum of values of said bits in the multi-bit digital signal.

2. (Previously Presented) The system of claim 1 wherein the first analog signal and the second analog signal are substantially equal to each other.

3 (Original) The system of claim 1 wherein the DAC comprises a switched capacitor DAC.

4. (Previously Presented) A method comprising:

receiving a multi-bit digital signal; and

generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal.

5. (Previously Presented) The method of claim 4 wherein the first analog signal and the second analog signal are substantially equal to one another.

6. (Original) The method of claim 5 wherein generating comprises:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal; and

connecting at least two of the plurality of capacitors to one another to share charge with one another.

7. (Previously Presented) A system comprising:

means for receiving a multi-bit digital signal; and

means for generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal.

8. (Previously Presented) The system of claim 7 wherein the first analog signal and the second analog signal are substantially equal to one another.

9. (Original) The system of claim7 wherein means for generating comprises a switched capacitor DAC.

10-15. (Cancelled).

16. (Original) A system comprising:

a binary weighted DAC; and

a segmented DAC, coupled to the binary weighted DAC, the segment DAC comprising a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, at least two of the plurality of sub DACs sharing charge with one another, and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

17. (Previously Presented) The system of claim 29 wherein the digital signal processing stage comprises

a scrambler.

18. (Previously Presented) A system as claimed in claim 17 wherein the number of bits in the multi-bit input to the DAC is greater than the number of bits in the multi-bit output of the scrambler.

19. (Previously Presented) The system of claim 18 wherein at least one of the bits of the multi-bit input to the scrambler is coupled to a first logic signal, and at least one of the bits of the multi-bit input to the DAC is coupled to a second logic signal having a logic state opposite a logic state of the first signal.

20. (Original) The system of claim 19 wherein there is a predetermined relationship between the first logic signal and the second logic signal.

21. (Original) The system of claim 19 wherein the first logic signal and the second logic signal do not change logic state .

22-26. (Cancelled).

27. (Original) A handset for a mobile communication system comprising:

an input stage that receives an input signal and outputs a multi-bit digital signal to a digital-to-analog conversion system that receives the multi-bit digital signal and outputs an analog signal indicative of a sum of values of bits in the multi-bit signal, and comprising:

a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associate bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, at least two of the plurality of sub DACs sharing charge with one another, and the switched capacitor network outputs at least one analog signal indicative of a sum of values of bits in the multi-bit signal.

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28 ~~29~~. (Previously Presented) A system comprising:

a digital signal processing stage that receives a multi-bit input and provides a multi-bit output; and

a switched capacitor DAC that receives a multi-bit input signal that includes the multi-bit output of the digital signal processing stage, the switched capacitor DAC having a plurality of

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sub DACs that each receive an associated amount of charge in response to the multi-bit input signal received by the DAC, the switched capacitor DAC having an operating state in which at least two of the plurality of sub DACs share charge with one another such that the associated charges are redistributed, and having an operating state in which the switched capacitor DAC outputs an analog signal that is indicative of the multi-bit input signal received by the switched capacitor DAC using less than all of the redistributed charge.

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~~30.~~ (Previously Presented) A digital to analog converter receives a first multi-bit digital signal and a second multi-bit digital signal ,and produces an analog output that is indicative of a product of the first multi-bit digital signal and the second multi-bit digital signal.

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~~31.~~ (Cancelled).

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~~32.~~ (Previously Presented) The system of claim 29 wherein each of the sub DACs has an associated portion of the redistributed charge and the at least one analog signal includes an analog signal that is indicative of and generated in response to the portion of the redistributed charge that is associated with one of the sub DACs.

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~~33.~~ (Previously Presented) A system comprising:

a digital signal processing stage that receives a multi-bit input and provides a multi-bit output; and

a switched capacitor DAC wherein the DAC comprises a switched capacitor network that receives a multi-bit input that includes the multi-bit output from the digital signal processing stage, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, the DAC having an operating state in which at least two of the plurality of sub DACs share charge with one another, and having an operating state in which less than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of bits in the multi-bit input received by the DAC.

33 ~~34~~. (Previously Presented) The system of claim ~~33~~ 32 wherein the DAC has an operating state in which only one of the plurality of sub DACs is connected to the output terminal and the switched capacitor network outputs one analog signal indicative of a sum of values of each bit in the multi-bit input to the DAC.

34 ~~35~~. (Previously Presented) The system of claim 1 wherein the DAC has a first circuit portion and a second circuit portion, and the first analog output signal is generated based on a signal from the first circuit portion, and the second analog output signal is generated based on a signal from the second circuit portion.

35 ~~36~~. (Previously Presented) The system of claim 1 wherein the DAC has a first sub DAC and a second sub DAC, the first analog output signal is generated based on a signal from the first sub DAC, and the second analog output signal is generated based on a signal from the second sub DAC.

36 ~~37~~. (Previously Presented) The system of claim 1 wherein the DAC has a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, the switched capacitor DAC having an operating state in which at least two of the plurality of sub DACs are operatively connected to at times share charge with one another, effecting a redistribution of charge upon which each has a redistributed amount of charge, the first analog output signal being generated based on the redistributed charge of one of the sub DACs, and the second analog signal being generated based the redistributed charge of another one of the sub DACs.

37 ~~38~~. (Previously Presented) The system of claim 1 wherein the DAC has a first output line and a second output line and the DAC has at least one operating state in which the first output line and the second output line are not connected to one another and the first analog output signal is output on the first output line, and at least one operating state in which the first output line and the second output line are not connected to one another and the second analog signal is output on the second output line.

38 ~~39~~. (Previously Presented) The system of claim 29 wherein the plurality of sub DACs each receive an associated bit of the multi-bit input signal, and each of sub DACs receives its associated amount of charge in response to the associated bit.

39 ~~40~~. (Previously Presented) The system of claim 29 wherein the associated amount of charge received by one of the plurality of sub DACs is equal to zero.

40 ~~41~~. (Previously Presented) The system of claim 39 wherein the associated bit of one of the plurality of sub DACs has a low logic state and the associated amount of charge received in response to the associated bit is equal to zero.